CADEKA
Amplify the Human Experience

CDK1305

10-bit, 40 MSPS 175mW A/D Converter

FEATURES

- 40 MSPS converter
- 175mW power dissipation
- On-chip track-and-hold
- Single +5V power supply
- TTL/CMOS outputs
- 5pF input capacitance
- Tri-state output buffers
- High ESD protection: 3,500V minimum
- Selectable +3V or +5V logic I/O

APPLICATIONS

- All high-speed applications where low power dissipation is required
- Video imaging
- Medical imaging
- Radar receivers
- IR imaging
- Digital communications

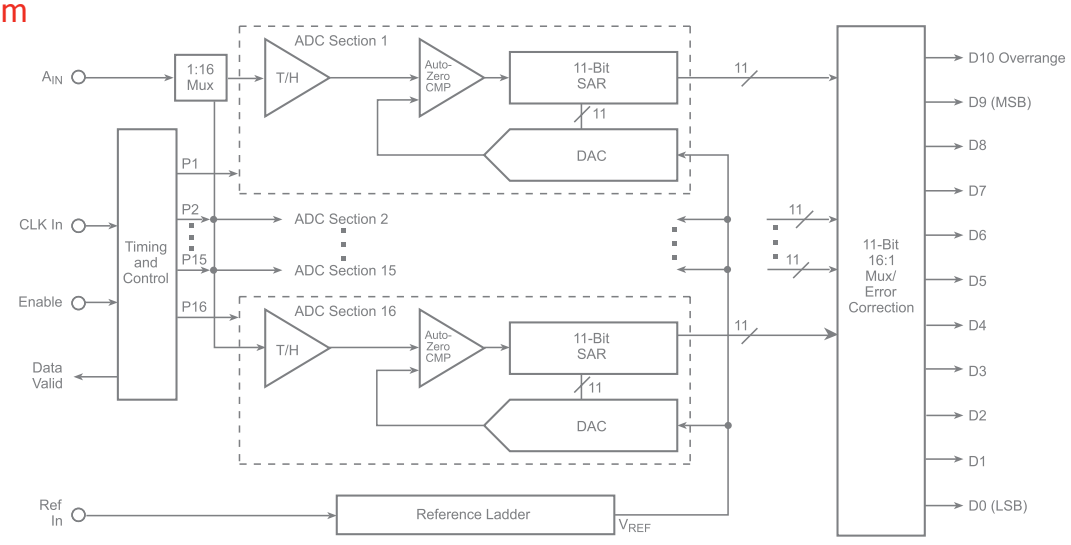
General Description

The CDK1305 is a 10-bit, low power analog-to-digital converter capable of minimum word rates of 40 MSPS. The on-chip track-and-hold function assures very good dynamic performance without the need for external components. The input drive requirements are minimized due to the CDK1305 low input capacitance of only 5pF.

Power dissipation is extremely low at only 175mW typical at 40 MSPS with a power supply of +5.0V. The digital outputs are +3V or +5V, and are user selectable. The CDK1305 is pin-compatible with an entire family of 10-bit, CMOS converters (CDK1304/05/06), which simplifies upgrades. The CDK1305 has incorporated proprietary circuit design* and CMOS processing technologies to achieve its advanced performance. Inputs and outputs are TTL/CMOS-compatible to interface with TTL/CMOS logic systems. Output data format is straight binary.

The CDK1305 is available in 28-lead SOIC and 32-lead small (7mm square) TQFP packages over the commercial temperature range.

Block Diagram



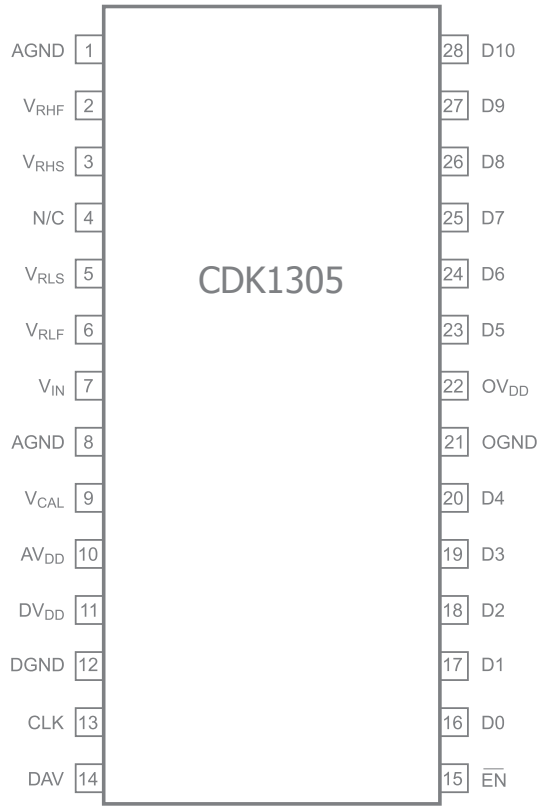
Ordering Information

Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CDK1305CSO28	SOIC-28	Yes	Yes	0°C to +70°C	Rail
CDK1305CSO28_Q	SOIC-28	No	No	0°C to +70°C	Rail
CDK1305CTQ32	TQFP-32	Yes	Yes	0°C to +70°C	Rail
CDK1305CTQ32_Q	TQFP-32	No	No	0°C to +70°C	Rail

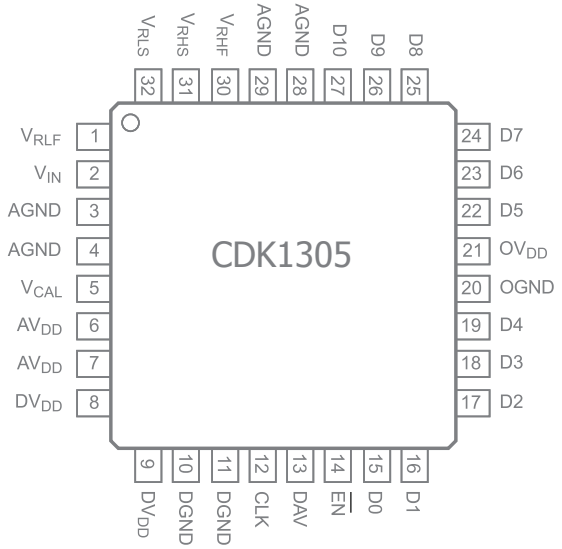
Moisture sensitivity level for SOIC-28 is MSL-1 and TQFP is MSL-3.

Pin Configuration

SOIC-28



TQFP-32



Pin Assignments

SOIC-28	TQFP-32	Pin Name	Description
1,8	3,4,28,29	AGND	Analog Ground
2	30	V_{RHF}	Reference High Force
3	31	V_{RHS}	Reference High Sense
5	32	V_{RLS}	Reference Low Sense
6	1	V_{RLF}	Reference Low Force
9	5	V_{CAL}	Calibration Reference
7	2	V_{IN}	Analog Input
10	6,7	AV_{DD}	Analog V_{DD}
11	8,9	DV_{DD}	Digital V_{DD}
12	10,11	DGND	Digital Ground
13	12	CLK	Input Clock f_{CLK} = FS (TTL)
15	14	$\overline{EN}$	Output Enable
16-20, 23-27	15-19, 22-26	D0-D9	Tri-State Data Output, (D0 = LSB)
28	27	D10	Tri-State Output Overrange
14	13	D_{AV}	Data Valid Output
22	21	OV_{DD}	Digital Output Supply
21	20	OGND	Digital Output Ground
4	–	N/C	No Connect

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltages			
AV_{DD}		+6	V
DV_{DD}		+6	V
Input Voltages			
Analog input	-0.5	AV_{DD} +0.5	V
V_{Ref}	0	AV_{DD}	V
CLK input		V_{DD}	V
AV_{DD} – DV_{DD}	-100	100	mV
AGND – DGND	-100	100	mV
Digital Outputs		10	mA

Reliability Information

Parameter	Min	Typ	Max	Unit
Storage Temperature Range	-65		+150	°C

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	0		+70	°C
Junction Temperature Range			+175	°C
Lead Temperature (soldering 10 seconds)			+300	°C

Electrical Characteristics

(T_A = T_{Min} to T_{Max}, AV_{DD} = DV_{DD} = OV_{DD} = +5V, V_{IN} = 0 to 4V, f_{clk} = 40 MSPS, V_{RHS} = 4V, V_{RLS} = 0V; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Resolution		10			bits
DC Performance						
DLE	Differential Linearity Error(1)		-0.5		+0.5	LSB
ILE	Integral Linearity Error(1)		-1.0		+1.0	LSB
	No Missing Codes		Guaranteed			
Analog Input						
	Input Voltage Range(1)		V_{RLS}		V_{RHS}	V
	Input Resistance(2)		50			kΩ
	Input Capacitance			5		pF
	Input Bandwidth	Small Signal		250		MHz
	Gain Error			±2.0		LSB
	Offset Error			±2.0		LSB
Reference Input						
	Resistance(1)		300	500	600	Ω
	Bandwidth	Small Signal		150		MHz
	Voltage Range	V_{RLS}(2)	0		2.0	V
		V_{RHS}(2)	3.0		AV_{DD}	V
		$V_{RHS} - V_{RLS}$		4.0		V
		$\Delta (V_{RHF} - V_{RHS})$		90		mV
		$\Delta (V_{RLS} - V_{RLF})$		75		mV
Reference Settling Time						
	V_{RHS}			15		CLK Cycle
	V_{RLS}			20		CLK Cycle
Conversion Characteristics						
	Maximum Conversion Rate(1)		40			MHz
	Minimum Conversion Rate(2)		2			MHz
	Pipeline Delay (Latency)(2)				12	CLK Cycle
	Aperture Delay Time			4.0		ns
	Aperture Jitter Time			30		ps_{pp}
Dynamic Performance						
ENOB	Effective Number of Bits	f_{IN} = 3.58MHz		8.5		Bits
		f_{IN} = 10.3MHz		8.3		Bits
SNR	Signal-to-Noise Ratio w/o Harmonics	f_{IN} = 3.58MHz(1)	52	54		dB
		f_{IN} = 10.3MHz(1)	51	52		dB
THD	Total Harmonic Distortion	f_{IN} = 3.58MHz(1), 9 distortion bins from 1024 pt FFT	55	61		dB
		f_{IN} = 10.3MHz(1), 9 distortion bins from 1024 pt FFT	52	53		dB
SINAD	Signal-to-Noise and Distortion	f_{IN} = 3.58MHz(1)	51	54		dB
		f_{IN} = 10.3MHz(1)	49	52		dB

Notes:

1. 100% production tested at +25°C.
2. Parameter is guaranteed (but not tested) by design and characterization data.

Electrical Characteristics

(T_A = T_{Min} to T_{Max}, AV_{DD} = DV_{DD} = OV_{DD} = +5V, V_{IN} = 0 to 4V, f_{clk} = 40 MSPS, V_{RHS} = 4V, V_{RLS} = 0V; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SFDR	Spurious Free Dynamic Range	f_{IN} = 1MHz		63		ps_{pp}
	Differential Phase			±0.3		deg
	Differential Gain			±0.3		%
Digital Inputs						
	Logic "1" Voltage(1)		2.0			V
	Logic "0" Voltage(1)				0.8	V
	Maximum Input Current Low(1)		-10		+10	µA
	Maximum Input Current High(1)		-10		+10	µA
	Input Capacitance			+5		pF
Digital Outputs						
	Logic "1" Voltage(1)	I_{OH} = 0.5mA	3.5			V
	Logic "0" Voltage(1)	I_{OL} = 1.6mA			0.4	V
T_R	Rise Time	15pF load		10		ns
T_F	Fall Time	15pF load		10		ns
	Output Enable to Data Output Delay	20pF load, T_A = 25°C		10		ns
		50pF load over temp		22		ns
Power Supply Requirements						
OV_{DD}	Digital Voltage Supply(2)		3.0		5.0	V
DV_{DD}			4.75	5.0	5.25	V
AV_{DD}			4.75	5.0	5.25	V
AI_{DD}	Digital Voltage Current(1)			17	22	mA
DI_{DD}				18	23	mA
	Power Dissipation(1)			175	225	mW

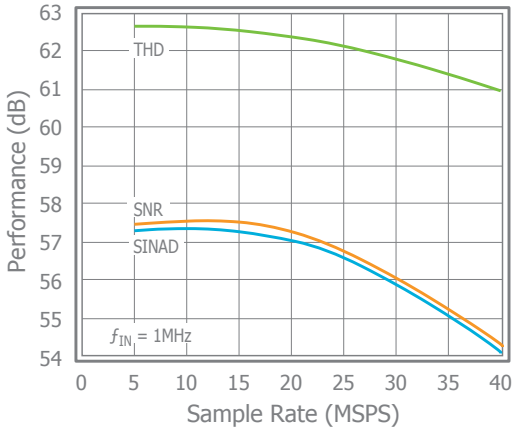
Notes:

1. 100% production tested at +25°C.
2. Parameter is guaranteed (but not tested) by design and characterization data.

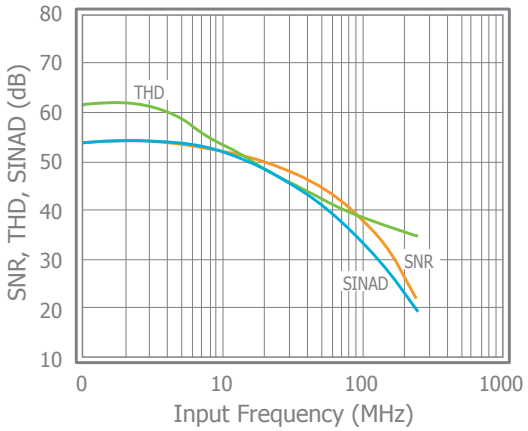
Typical Performance Characteristics

(T_A = T_{Min} to T_{Max}, AV_{DD} = DV_{DD} = OV_{DD} = +5V, V_{IN} = 0 to 4V, f_{clk} = 40 MSPS, V_{RHS} = 4V, V_{RLS} = 0V; unless otherwise noted)

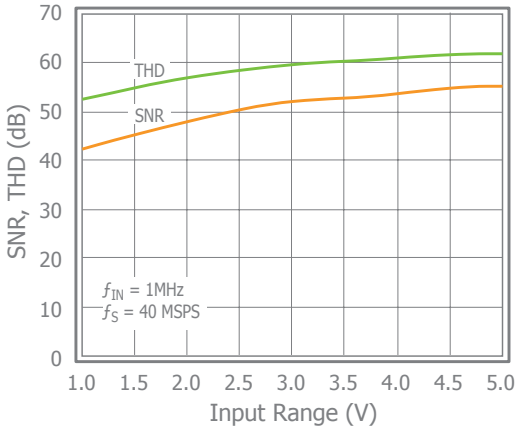
Performance vs. Sample Rate



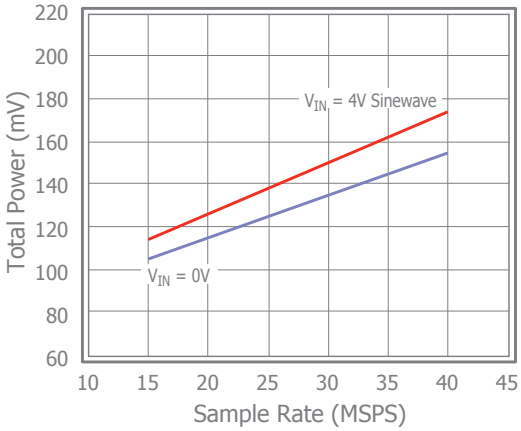
SNR, THD, SINAD vs. Input Freq.



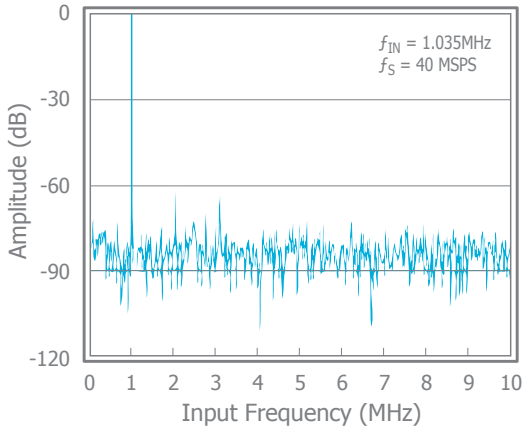
SNR, THD vs. Input Range



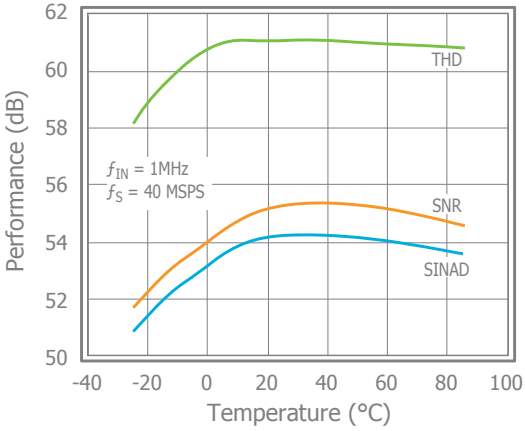
Power Dissipation vs. Sample Rate



Spectral Response



Performance vs. Temperature



Specification Definitions

Aperture Delay

Aperture delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

Aperture Jitter

The variations in aperture delay for successive samples.

Differential Gain (DG)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential gain is the maximum variation in the sampled sine wave amplitudes at these DC levels.

Differential Phase (DP)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential phase is the maximum variation in the sampled sine wave phases at these DC levels.

Effective Number Of Bits (ENOB)

SINAD = 6.02N + 1.76, where N is equal to the effective number of bits.

$$N = \frac{SINAD - 1.76}{6.02}$$

Input Bandwidth

Small signal (50mV) bandwidth (3dB) of analog input stage.

Differential Linearity Error (DLE)

Error in the width of each code from its theoretical value. (Theoretical = $V_{FS}/2^N$)

Integral Linearity Error (ILE)

Linearity error refers to the deviation of each individual code (normalized) from a straight line drawn from –FS through +FS. The deviation is measured from the edge of each particular code to the true straight line.

Output Delay

Time between the clock's triggering edge and output data valid.

Overvoltage Recovery Time

The time required for the ADC to recover to full accuracy after an analog input signal 125% of full scale is reduced to 50% of the full-scale value.

Signal-To-Noise Ratio (SNR)

The ratio of the fundamental sinusoid power to the total noise power. Harmonics are excluded.

Signal-To-Noise And Distortion (SINAD)

The ratio of the fundamental sinusoid power to the total noise and distortion power.

Total Harmonic Distortion (THD)

The ratio of the total power of the first 9 harmonics to the power of the measured sinusoidal signal.

Spurious Free Dynamic Range (SFDR)

The ratio of the fundamental sinusoidal amplitude to the single largest harmonic or spurious signal.

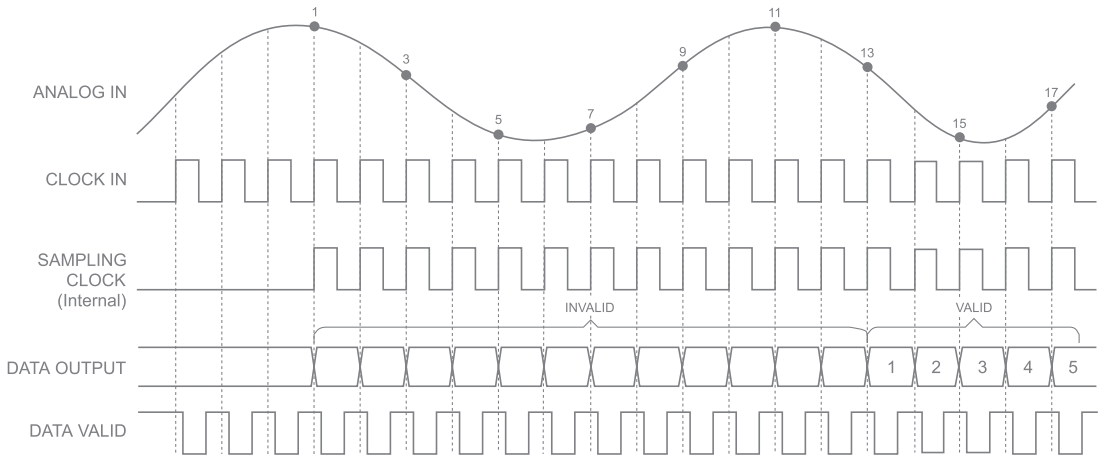


Figure 1. Timing Diagram 1

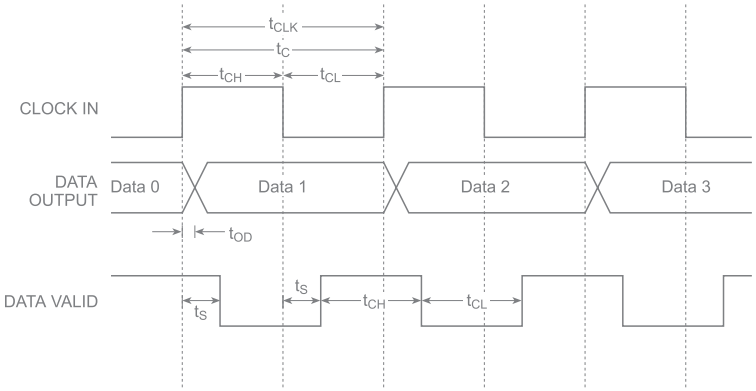
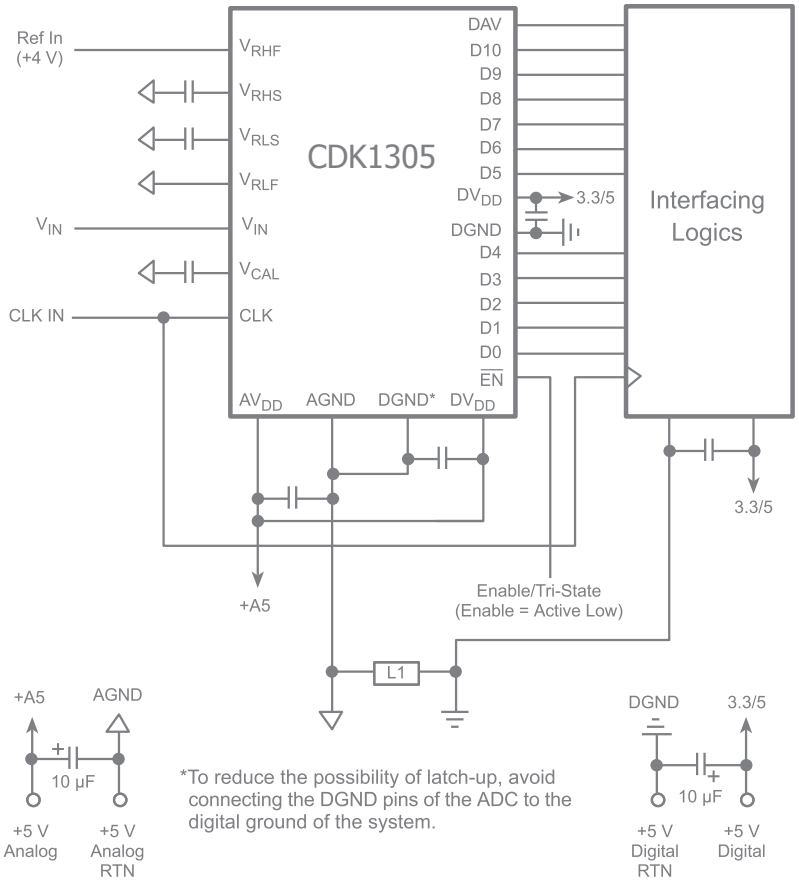


Figure 2. Timing Diagram 2

Table 1. Timing Parameters

Description	Sym	Min	Typ	Max	Units
Conversion Time	t_C	t_{CLK}			ns
CLK Period	t_{CLK}	40			ns
CLK High Duty Cycle	t_{CH}	40	50	60	%
CLK Low Duty Cycle	t_{CL}	40	50	60	%
CLK to Output Delay (15pF load)	t_{OD}		17		ns
CLK to DAV	t_S		10		ns



NOTES: 1) L1 is to be located as closely to the device as possible.
2) All capacitors are 0.1 µF surface-mount unless otherwise specified.
3) L1 is a 10 µH inductor or a ferrite bead.

Figure 3. Typical Interface Circuit Diagram

Typical Interface Circuit

Very few external components are required to achieve the stated device performance. Figure 2 shows the typical interface requirements when using the CDK1305 in normal circuit operation. The following sections provide descriptions of the major functions and outline critical performance criteria to consider for achieving the optimal device performance.

Power Supplies And Grounding

Cadeka suggests that both the digital and the analog supply voltages on the CDK1305 be derived from a single analog supply as shown in Figure 2. A separate digital supply should be used for all interface circuitry. Cadeka suggests using this power supply configuration to prevent a possible latch-up condition on powerup.

Operating Description

The general architecture for the CMOS ADC is shown in the Block Diagram. The design contains 16 identical successive approximation ADC sections, all operating in parallel, a 16-phase clock generator, an 11-bit 16:1 digital output multiplexer, correction logic, and a voltage reference generator that provides common reference levels for each ADC section.

The high sample rate is achieved by using multiple SAR ADC sections in parallel, each of which samples the input signal in sequence. Each ADC uses 16 clock cycles to complete a conversion. The clock cycles are allocated as shown in Table 2.

Table 2. Clock Cycles

Clock	Operation
1	Reference zero sampling
2	Auto-zero comparison
3	Auto-calibrate comparison
4	Input sample
5-15	11-bit SAR conversion
16	Data transfer

The 16-phase clock, which is derived from the input clock, synchronizes these events. The timing signals for adjacent ADC sections are shifted by one clock cycle so that the analog input is sampled on every cycle of the input clock by exactly one ADC section. After 16 clock periods, the timing cycle repeats. The latency from analog input sample to the corresponding digital output is 12 clock cycles.

- Since only 16 comparators are used, a huge power savings is realized.
- The auto-zero operation is done using a closed loop system that uses multiple samples of the comparator's response to a reference zero.
- The auto-calibrate operation, which calibrates the gain of the MSB reference and the LSB reference, is also done with a closed loop system. Multiple samples of the gain error are integrated to produce a calibration voltage for each ADC section.
- Capacitive displacement currents, which can induce sampling error, are minimized since only one comparator samples the input during a clock cycle.
- The total input capacitance is very low since sections of the converter that are not sampling the signal are isolated from the input by transmission gates.

Voltage Reference

The CDK1305 requires the use of a single external voltage reference for driving the high side of the reference ladder. It must be within the range of 3V to 5V. The lower side of the ladder is typically tied to AGND (0.0V), but can be run up to 2.0V with a second reference. The analog input voltage range will track the total voltage difference measured between the ladder sense lines, V_{RHS} and V_{RLS}.

Force and sense taps are provided to ensure accurate and stable setting of the upper and lower ladder sense line voltages across part-to-part and temperature variations. By using the configuration shown in Figure 4, offset and gain errors of less than ±2 LSB can be obtained.

In cases where wider variations in offset and gain can be tolerated, V_{REF} can be tied directly to V_{RHF}, and AGND can be tied directly to V_{RLF} as shown in Figure 5. Decouple force and sense lines to AGND with a 0.01µF capacitor (chip cap preferred) to minimize high-frequency noise injection.

If this simplified configuration is used, the following considerations should be taken into account. The reference ladder circuit shown in Figure 5 is a simplified representation of the actual reference ladder with force and sense taps shown. Due to the actual internal structure of the ladder, the voltage drop from V_{RHF} to V_{RHS} is not equivalent to the voltage drop from V_{RLF} to V_{RLS}.

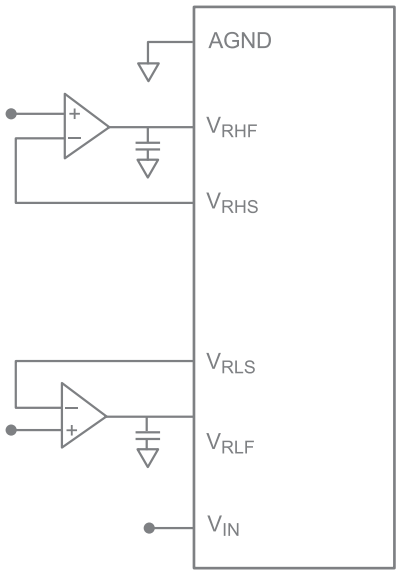


Figure 4. Ladder Force/Sense Circuit

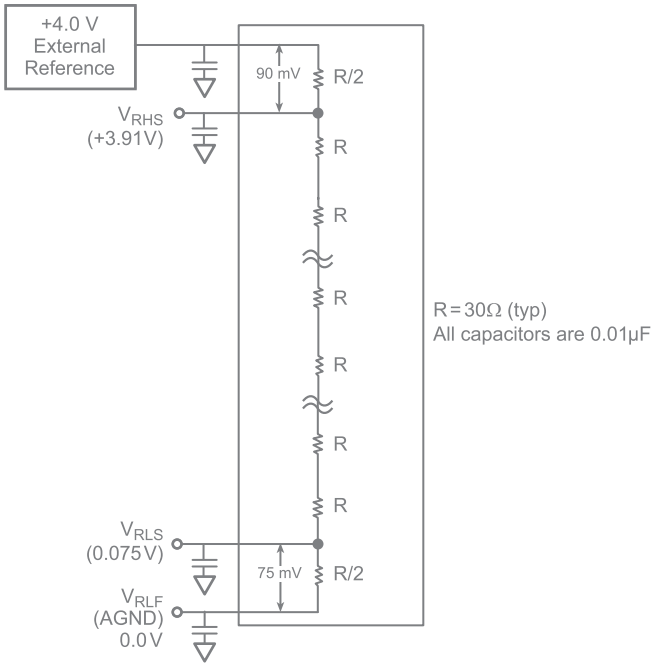


Figure 5. Reference Ladder Circuit

Typically, the top side voltage drop for V_{RHF} to V_{RHS} will equal:

$$V_{RHF} - V_{RHS} = 2.25\ \%\ \text{of}\ (V_{RHF} - V_{RLF})\ \text{(typical)}$$

and the bottom side voltage drop for V_{RLS} to V_{RLF} will equal:

$$V_{RLS} - V_{RLF} = 1.9\ \%\ \text{of}\ (V_{RHF} - V_{RLF})\ \text{(typical)}$$

Figure 5 shows an example of expected voltage drops for a specific case. V_{REF} of 4.0V is applied to V_{RHF}, and V_{RLF} is tied to AGND. A 90mV drop is seen at V_{RHS} (= 3.91V), and a 75mV increase is seen at V_{RLS} (= 0.075V).

Analog Input

V_{IN} is the analog input. The input voltage range is from V_{RLS} to V_{RHS} (typically 4.0V) and will scale proportionally with respect to the voltage reference. (See Voltage Reference section.)

The drive requirements for the analog inputs are very minimal when compared to most other converters due to the CDK1305 extremely low input capacitance of only 5pF and very high input resistance of 50kΩ.

The analog input should be protected through a series resistor and diode clamping circuit as shown in Figure 7.

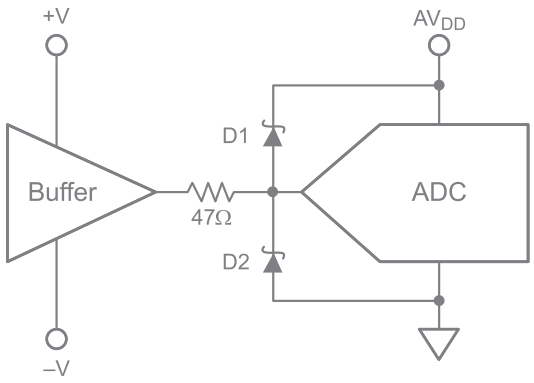


Figure 6. Recommended Input Protection Circuit

Calibration

The CDK1305 uses an auto-calibration scheme to ensure 10-bit accuracy over time and temperature. Gain and offset errors are continually adjusted to 10-bit accuracy during device operation. This process is completely transparent to the user.

Upon powerup, the CDK1305 begins its calibration algorithm. In order to achieve the calibration accuracy required, the offset and gain adjustment step size is a fraction of a 10-bit LSB. Since the calibration algorithm is an oversampling process, a minimum of 10,000 clock cycles are required. This results in a minimum calibration time upon powerup of 250µs (for a 40MHz clock). Once calibrated, the CDK1305 remains calibrated over time and temperature.

Since the calibration cycles are initiated on the rising edge of the clock, the clock must be continuously applied for the CDK1305 to remain in calibration.

Input Protection

All I/O pads are protected with an on-chip protection circuit shown in Figure 6. This circuit provides ESD robustness to 3.5kV and prevents latch-up under severe discharge conditions without degrading analog transition times.

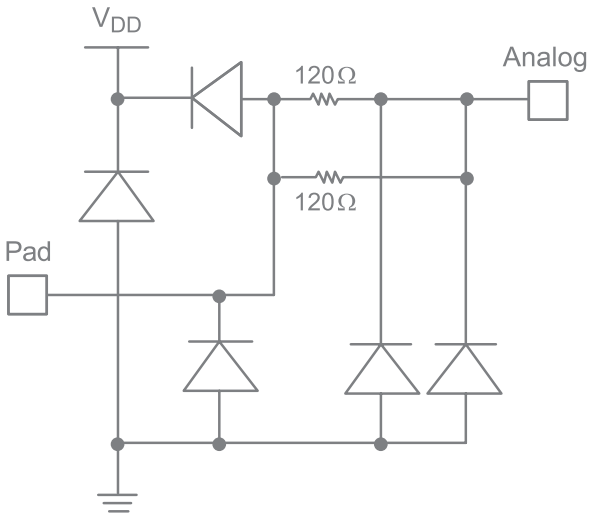


Figure 7. On-Chip Protection Circuit

Power Supply Sequencing Considerations

All logic inputs should be held low until power to the device has settled to the specific tolerances. Avoid power decoupling networks with large time constants that could delay VDD power to the device.

Clock Input

The CDK1305 is driven from a single-ended TTL-input clock. Because the pipelined architecture operates on the rising edge of the clock input, the device can operate over a wide range of input clock duty cycles without degrading the dynamic performance.

Digital Outputs

The digital outputs (D0–D10) are driven by a separate supply (OVDD) ranging from +3 V to +5 V. This feature makes it possible to drive the CDK1305 TTL/CMOS compatible outputs with the user's logic system supply. The format of the output data (D0–D9) is straight binary. (See Table 3.) The outputs are latched on the rising edge of CLK. These outputs can be switched into a tri-state mode by bringing EN high.

Table 3. Output Data Information

Analog Input	Overrange D10	Output Code D9-D0
+F.S. + 1/2 LSB	1	1 1 1 1 1 1 1 1 1 1
+F.S. –1/2 LSB	0	1 1 1 1 1 1 1 1 1Ø
+1/2 F.S.	0	ØØ ØØØØ ØØØØ
+1/2 LSB	0	0 0 0 0 0 0 0 0 0 Ø
0.0V	0	0 0 0 0 0 0 0 0 0 0

(Ø indicates the flickering bit between logic 0 and 1.)

Overrange Output

The Overrange Output (D10) is an indication that the analog input signal has exceeded the positive fullscale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1.

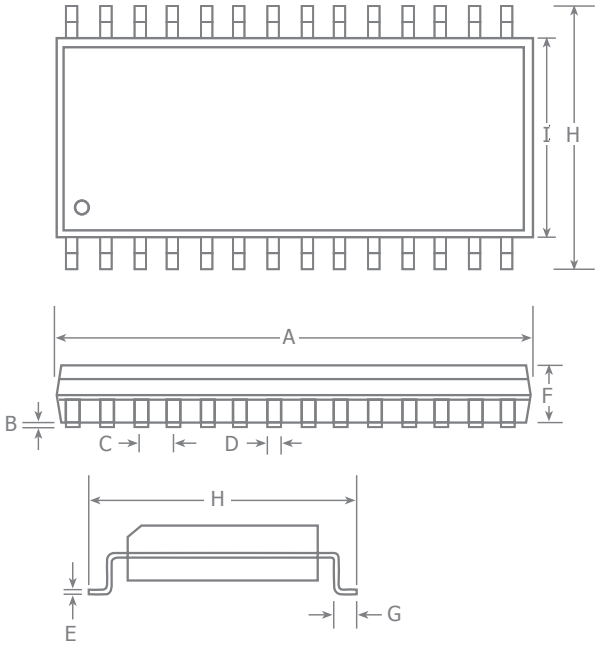
This feature makes it possible to include the CDK1305 in higher resolution systems.

Evaluation Board

The TBD evaluation board is available to aid designers in demonstrating the full performance of the CDK1305. This board includes a reference circuit, clock driver circuit, output data latches, and an on-board reconstruction of the digital data. An application note describing the operation of this board, as well as information on the testing of the CDK1305, is also available. Contact the factory for price and availability.

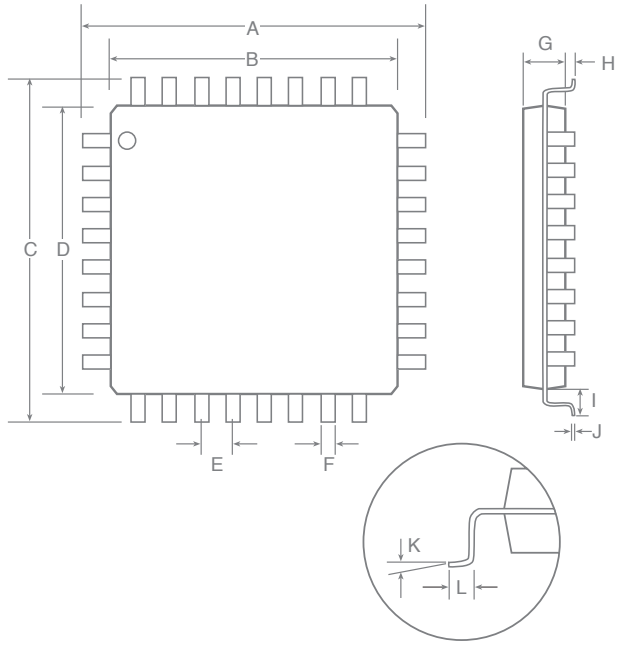
Mechanical Dimensions

SOIC-28 Package



	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.699	0.709	17.75	18.01
B	0.005	0.011	0.13	0.28
C	0.050 Typ		1.27 BSC	
D	0.018 Typ		0.46 BSC	
E	0.0077	0.0083	0.20	0.21
F	0.090	0.096	2.29	2.44
G	0.031	0.039	0.79	0.99
H	0.396	0.416	10.06	10.57
I	0.286	0.292	7.26	7.42

TQFP-32 Package



	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.346	0.362	8.80	9.20
B	0.272	0.280	6.90	7.10
C	0.346	0.362	8.80	9.20
D	0.272	0.280	6.90	7.10
E	0.031 Typ		0.80 BSC	
F	0.012	0.016	0.30	0.40
G	0.053	0.057	1.35	1.45
H	0.002	0.006	0.05	0.15
I	0.037	0.041	0.95	1.05
J		0.007		0.17
K	0°	7°	0°	7°
L	0.020	0.030	0.50	0.75

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